CLAIMS

What is claimed is:

1. A probe card assembly for electrically communicating test data between a semiconductor test apparatus and a semiconductor device under test, said probe card assembly comprising:

a substrate configured to electrically contact said semiconductor tester apparatus,

a plurality of probes configured to electrically contact said semiconductor device under test, said plurality of probes located to a first side of said substrate, and

a daughter card secured to a second side of said substrate in spaced relationship to said substrate, said daughter card being substantially coplanar to said substrate.

2. The probe card assembly of claim 1 further comprising an electric circuit at least a portion of which is disposed on said daughter card.

3. The probe card assembly of claim 2, wherein said electric circuit includes active circuit elements.

4. The probe card assembly of claim 2, wherein said electric circuit is configured to enhance test capabilities of said semiconductor test apparatus.

5. The probe card assembly of claim 2, wherein said electric circuit is configured to customize at least a portion of said test data to test needs of said semiconductor device under test.

Sub B1

6. The probe card assembly of claim 5, wherein said test data comprises test signals generated by said semiconductor test apparatus and said electric circuit customizes at least a portion of said test signals.

7. The probe card assembly of claim 5, wherein said test data comprises response signals generated by said semiconductor device under test and said electric circuit customizes at least a portion of said response signals.

8. The probe card assembly of claim 1 further comprising a plurality of said daughter cards.

9. The probe card assembly of claim 8, wherein said plurality of daughter cards are disposed in stacked relationship to each other.

10. The probe card assembly of claim 8 further comprising an electric circuit at least a portion of which is disposed on each of said plurality of daughter cards.

11. The probe card assembly of claim 10, wherein said electric circuit includes active circuit elements.

12. The probe card assembly of claim 10, wherein said electric circuit is configured to enhance test capabilities of said semiconductor test apparatus.

13. The probe card assembly of claim 10, wherein said electric circuit is configured to customize at least a portion of said test data to test needs of said semiconductor device under test.

14. The probe card assembly of claim 13, wherein said test data comprises test signals generated by said semiconductor test apparatus and said electric circuit customizes at least a portion of said test signals.

15. The probe card assembly of claim 13, wherein said test data comprises response signals generated by said semiconductor device under test and said electric circuit customizes at least a portion of said response signals.

16. The probe card assembly of claim 8, wherein said plurality of daughter cards includes at least three daughter cards.

17. The probe card assembly of claim 16 further comprising an electric circuit at least a portion of which is disposed on each of said at least three daughter cards.

18. The probe card assembly of claim 16, wherein said at least three daughter cards are disposed in stacked relationship to each other.

Sub B1

19. A method of making a probe card assembly, said method comprising:

providing a substrate including a plurality of tester contacts,

securing a plurality of probes to a first side of said substrate, said probes configured to electrically contact a semiconductor device under test, and

securing a daughter card to a second side of said substrate in spaced relationship to said substrate, said daughter card being substantially coplanar to said substrate.

20. The method of claim 19 further comprising:

providing an electric circuit, and

disposing at least a portion of said electric circuit on said daughter card.

21. The method of claim 20, wherein said electric circuit includes active circuit elements.

22. The method of claim 20, wherein said electric circuit is configured to enhance test capabilities of said semiconductor test apparatus.

23. The method of claim 20, wherein said electric circuit is configured to customize test data to test needs of said semiconductor device under test.

24. The method of claim 23, wherein said test data comprises test signals to be input into said semiconductor device under test and said electric circuit customizes at least a portion of said test signals.

Sub B1

25. The method of claim 23, wherein said test data comprises response signals generated by said semiconductor device under test and said electric circuit customizes at least a portion of said response signals.

26. The method of claim 19 further comprising securing a plurality of said daughter cards to said substrate.

27. The method of claim 26 further comprising securing said plurality of daughter cards to said substrate in stacked relationship to each other.

28. The method of claim 26 further comprising:

providing an electric circuit, and

disposing at least a portion of said electric circuit on each of said plurality of daughter cards.

29. The method of claim 28, wherein said electric circuit includes active circuit elements.

30. The method of claim 28, wherein said electric circuit is configured to enhance test capabilities of said semiconductor test apparatus.

Sub B1

31. The method of claim 28, wherein said electric circuit is configured to customize test data to test needs of said semiconductor device under test.

32. The method of claim 31, wherein said test data comprises test signals to be input into said semiconductor device under test and said electric circuit customizes at least a portion of said test signals.

33. The method of claim 31, wherein said test data comprises response signals generated by said semiconductor device under test and said electric circuit customizes at least a portion of said response signals.

34. The method of claim 26, wherein said plurality of daughter cards includes at least three daughter cards.

35. The method of claim 34 further comprising:

providing an electric circuit, and

disposing at least a portion of said electric circuit on each of said at least three daughter cards.

36. The method of claim 34 further comprising securing each of said at least three daughter cards to said substrate in stacked relationship to each other.

37. A probe card assembly made using the process of claim 19.

38. A probe card assembly made using the process of claim 20.

39. A probe card assembly made using the process of claim 22.

40. A probe card assembly made using the process of claim 26.

41. A probe card assembly made using the process of claim 30.

42. A probe card assembly comprising:

printed circuit means for electrically communicating with a semiconductor tester apparatus,

contact means for electrically communicating with a semiconductor device under test, said contact means being secured to a first surface of said printed circuit means, and

daughter card means for physically supporting at least a portion of an electric circuit, said daughter card means secured to a second surface of said printed circuit means and being substantially coplanar to said printed circuit means.

43. The probe card assembly of claim 42, wherein said daughter card means comprises a plurality of daughter cards in stacked relationship to each other, each of said plurality of daughter cards being substantially coplanar to said printed circuit means.

Sub B1

44. The probe card assembly of claim 43, wherein said plurality of daughter cards includes at least three daughter cards.

45. The probe card assembly of claim 42, wherein said electric circuit comprises processing means for processing test data for testing said semiconductor device under test.

46. The probe card assembly of claim 45, wherein said processing means enhances test capabilities of said semiconductor test apparatus.

47. The probe card assembly of claim 45, wherein said processing means customizes said test data to meet test needs of said semiconductor device under test.

48. The probe card assembly of claim 47, wherein said test data comprises test signals to be input into said semiconductor device under test and said processing means customizes at least a portion of said test signals.

49. The probe card assembly of claim 47, wherein said test data comprises response signals generated by said semiconductor device under test and said processing means customizes at least a portion of said response signals.

Sub B1

50. A probe card assembly for electrically communicating test data between a semiconductor test apparatus and a semiconductor device under test, said probe card assembly comprising:

a printed circuit board configured to electrically contact said semiconductor tester apparatus,

a plurality of probes configured to electrically contact said semiconductor device,

a daughter card secured to said printed circuit board in spaced relationship to said printed circuit board, said daughter card being substantially coplanar to said printed circuit board, and

an electric circuit configured to enhance test capabilities of said semiconductor test apparatus, at least a portion of said electric circuit being disposed on said daughter card.

51. The probe card assembly of claim 50 further comprising a plurality of said daughter cards.

52. The probe card assembly of claim 51, wherein said daughter cards are disposed in stacked relationship to each other.

53. The probe card assembly of claim 51, wherein said plurality of daughter cards includes at least two daughter cards.

54. The probe card assembly of claim 51, wherein said plurality of daughter cards includes at least three daughter cards.

55. The probe card assembly of claim 50, wherein said electric circuit enhances test capabilities of said semiconductor test apparatus by processing at least a portion of said test data.

56. The probe card assembly of claim 55, wherein said test data comprises test signals generated by said semiconductor tester apparatus and said electric circuit processes at least a portion of said test signals.

57. The probe card assembly of claim 55, wherein said test data comprises response signals generated by said semiconductor device and said electric circuit processes at least a portion of said response signals.